A Mathematical Guideline for Designing an AC-DC LLC Converter with PFC

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Abstract — **Although LLC topology has been applied to AC-DC power supplies as a Power Factor Correction (PFC) converter in the literature, there is no publications present intuitive equations that simplify LLC designing in order to meet the PFC gain requirements. In this paper, a mathematical design guideline is derived for LLC PFC converter applications, proving that by carefully designing the resonant tank gain at parallel resonant frequency at the peak AC voltage higher than 1, its gain will meet the PFC requirement for other AC voltages and result in a successful single-stage PFC design with power factor over 0.99. The guideline is extended to offline wide input and output voltage LLC PFC applications. A 240-Watt prototype of a single-stage LLC LED driver with PFC has been built to verify the feasibility of the proposed design guideline.**

Keywords — AC-DC Converter; PFC; LLC; Single-Stage; Resonant Converter

I. INTRODUCTION

Massive research have been attracted and new topologies have been studied on AC-DC power supply and its control strategy [1-6], LLC topology is still popularly used as the second stage converter to provide galvanic isolation and output voltage/current regulation [3, 4]. However, all the power is processed twice, which severely sacrifices the total efficiency and power density. To overcome this disadvantage, single-stage resonant solutions with PFC were discussed in [7-10]. The LLC resonant topology has been applied to a PFC converter in [7, 8] and then extended to an LED driver application in [9], resulting in power supplies with higher efficiency and a reduced profile. However, the primary switches operate at an asymmetrical duty ratio in the this article, which not only results in control and driving circuit complexity, but also introduces third harmonics into the input current, sacrificing the optimal power factor performance. In [10], using the rectifier-compensated fundamental-mode approximation method, the feasibility of the LLC topology working as a PFC converter is proven with 50% duty cycle switch operation. However, there is still no intuitive mathematical design guideline to help engineers quickly design the LLC converter to achieve the power factor correction without over-designing the gain. In this paper, a peak-gain-based mathematical model is proposed for an LLC converter that will achieve power factor correction and also guarantee enough gain for the entire line voltage range.

II. LLC RESONANT CONVERTER DESIGN GUIDELINE FOR PFC

A. LLC Resonant Converter Voltage Gain Review

The half-bridge LLC resonant converter prototype is shown in Fig. 1. The operating frequency range of the LLC PFC is defined as $f_p \leq f_s \leq f_r$, where below-resonance operation is preferred to ensure the inductive impedance characteristics of the LLC resonant tank, so that the soft switching can be achieved in both primary side switches and secondary diodes.
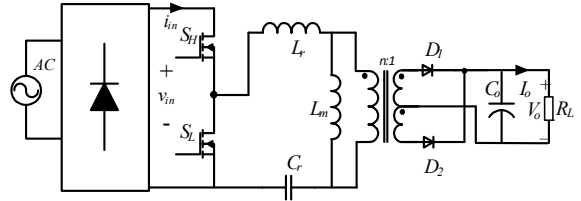

Fig. 1. Prototype of Half-Bridge LLC Power Factor Correction Circuit

The maximum switching frequency is set at the series resonant frequency f_r, expressed in (1). The quality factor Q, the inductance ratio K, the normalized switching frequency f_n and the total gain of the converter M_{LLC_total} are expressed in (2) to (5) [11-13] and n is the transformer's turns ratio.

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (1)$$

$$Q = \frac{\pi^2}{8n^2} \cdot \sqrt{\frac{L_r}{C_r}} \cdot \frac{I_{out}}{V_{out}} = \frac{\pi^2}{8n^2} \cdot \sqrt{\frac{L_r}{C_r}} \cdot \frac{1}{R_{out}} \quad (2)$$

$$K = \frac{L_m}{L_r} \quad (3)$$

$$f_n = \frac{f_r}{f_s} \quad (4)$$

$$M_{LLC\_total} = \frac{1}{2n} \cdot \frac{1}{\sqrt{\left[1 + \frac{1}{K}\left(1 - \frac{1}{f_n^2}\right)\right]^2 + \left[\left(f_n - \frac{1}{f_n}\right)Q\right]^2}} \quad (5)$$

B. Single-Stage PFC Gain Requirement Analysis

Fig. 2 plots the required voltage gain, $G_{req}(\theta)$, for an LLC converter in PFC mode, according to (6).
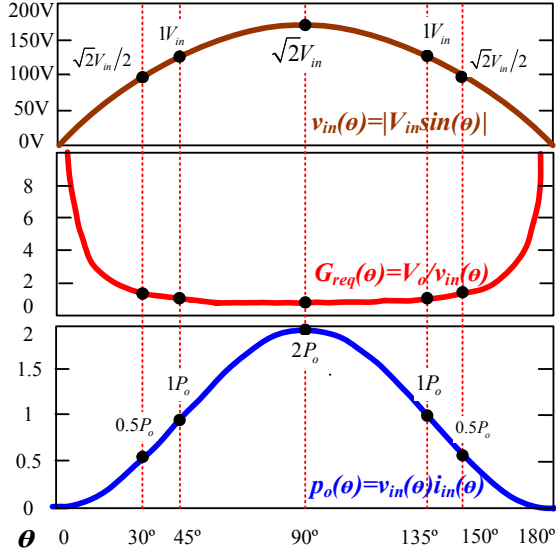
Fig. 2. Single-stage LLC PFC gain requirement

Fig. 3. Normalized LLC tank gain at parallel resonant frequency under different load, R_{out}

It is observed that $G_{req}(\theta)$ to achieve power factor correction is different at each time instant, while the LLC converter output power $p_{out}(\theta)$ is also changing as per (7).

$$G_{req}(\theta) = \frac{V_{out}}{v_{in}(\theta)} = \frac{V_{out}}{\sqrt{2}V_{in\_rms}\sin(\theta)} \quad (6)$$

$$p_{out}(\theta) = p_{in}(\theta) = v_{in}(\theta)i_{in}(\theta)$$
$$= 2I_{in\_rms}V_{in\_rms}(\sin(\theta))^2 = 2(\sin(\theta))^2 P_o \quad (7)$$

Assuming the AC input voltage is 120VRMS: at 90°, the LLC should provide two times the steady state output power ($P_{pk} = 2P_o$). At this time, the v_{in} is at peak V_{in_pk}=120V×1.414, which is good for providing higher output power. At 45°, the LLC should provide the output power (P_o), but v_{in} is 120V×1.414×sin(45°) =120V. The LLC converter should generate V_o at 120V input at output power level of P_o. At 30°, the $v_{in} = 0.5V_{in\_pk}$, and $i_{in} = 0.5I_{pk}$, the output power is $0.25P_{pk} = 0.5P_o$. Therefore, the LLC converter should provide V_o at the output power level of $0.5P_o$. In order to achieve high power factor correction performance, the LLC converter must achieve different gains at different input voltages.

For PFC application, the output voltage is usually a constant. When P_{out} decreases, R_{out} also linearly increases. Fig. 3 plots the normalized LLC tank gain at parallel frequency under different load (R_{out} ranges from 1 to 12). featuring an increasing gain when the R_{out} is increasing, this changing trend is in agreement with the PFC gain requirement as shown in Fig. 2. Therefore, LLC resonant converter is a potential candidate for single-stage PFC operation topology. The results from (1) to (5) will be used later to derive the design rule for the LLC converter in PFC mode.
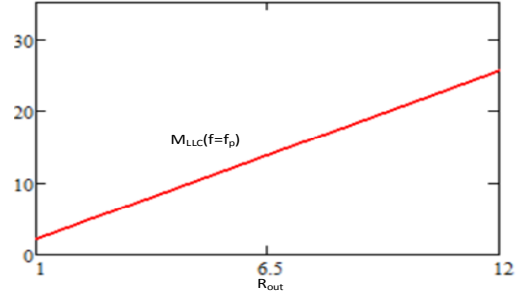
C. Derivation of the LLC Resonant Converter Design Guideline for PFC

The entire LLC PFC design guideline is composed of two parts: the transformer turns ratio design, and the LLC resonant tank design.

1) Transformer Turns Ratio Design Guideline

According to (6) and (7), the minimum gain requirement for a PFC design $G_{req}^{min}(\theta)$ occurs at $\theta=\pi/2$, when the instantaneous output power is equal to twice the average output power, $2P_o$. The minimum gain of the LLC resonant tank in the inductive operating range occurs at the series resonant frequency, f_r. Therefore, the total gain of the LLC converter at f_r is intentionally designed to be equal to the minimum gain requirement of the PFC converter in (8) and the resulting turns ratio is expressed in (9).

$$G_{req}^{min}(\theta) = G_{req}(\theta = \frac{\pi}{2})$$
$$= \frac{V_{out}}{\sqrt{2}V_{in\_rms}\sin(\frac{\pi}{2})} = \frac{V_{out}}{\sqrt{2}V_{in\_rms}} \quad (8)$$

$$n = \frac{N_{pri}}{N_{sec}} = \frac{V_{in\_RMS}}{\sqrt{2}V_{out}} \quad (9)$$

2) LLC Resonant Tank Design Guideline

In PFC mode, the quality factor Q_{pfc} changes with θ. Derived from (2), the θ-dependent quality factor, $Q_{pfc}(\theta)$ is shown in (10), where Q_{full_load} in (11) is the full load quality factor when the LLC resonant converter is working at the PFC average power P_o, and is a constant value. The total gain of the LLC resonant converter in PFC mode is shown in (12).

$$Q_{pfc}(\theta) = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}(\theta)} = 2(\sin(\theta))^2 \frac{\sqrt{\frac{L_r}{C_r}}}{R_{oe\_full\_load}} \quad (10)$$
$$= 2(\sin(\theta))^2 Q_{full\_load}$$

$$Q_{full\_load} = \frac{\pi^2}{8n^2} \cdot \sqrt{\frac{L_r}{C_r}} \cdot \frac{I_{out}}{V_{out}}$$
$$= \frac{\pi^2}{4} \frac{P_{out}}{V_{in\_RMS}^2} \cdot \sqrt{\frac{L_r}{C_r}} \quad (11)$$

$$M_{LLC\_total}(f_s,\theta)=\frac{1}{2n}\cdot M_{LLC}(f_s,\theta)$$

$$=\frac{1}{2n}\cdot\frac{1}{\sqrt{\left[1+\frac{1}{K}\left(1-\frac{f_r^2}{f_s^2}\right)\right]^2+4(\sin\theta)^4\left[\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)Q_{full\_load}\right]^2}} \qquad (12)$$

$$M_{LLC\_total}(f_s=f_p,\theta)=\frac{1}{2n}\cdot M_{LLC}(f_s=f_p,\theta)$$

$$=\frac{1}{2n}\cdot\frac{1}{\sqrt{\left[1+\frac{1}{K}\left(1-\frac{f_r^2}{f_p^2}\right)\right]^2+4(\sin\theta)^4\left[\left(\frac{f_p}{f_r}-\frac{f_r}{f_p}\right)Q_{full\_load}\right]^2}} \qquad (13)$$

Then the total gain of the LLC resonant converter at the parallel resonant frequency, $f_s=f_p$, is derived in (13). With the definitions of f_p in (14) and K in (3), (13) is simplified into (15).

$$f_p=\frac{1}{2\pi\sqrt{(L_m+L_r)C_r}} \qquad (14)$$

$$M_{LLC\_total}\left(f_s=f_p,\theta\right)=\frac{1}{2n}M_{LLC}\left(f_s=f_p,\theta\right)$$

$$=\frac{1}{2n\cdot(\sin\theta)^2\sqrt{\left(\frac{K^2}{1+K}\right)}\cdot 2Q_{full\_load}} \qquad (15)$$

If the LLC resonant tank gain for the peak input voltage ($\theta=\pi/2$) at the parallel resonant frequency $M_{LLC}(f_s=f_p,\theta=\pi/2)$ is designed equal to or higher than 1, as shown in (16), the resulting total LLC resonant converter gain can be then derived from (9), (11) and (15), and is shown in (17). Since the inequality of $1/(\sin\theta)^2 \geq 1/(\sin\theta)$ is always valid for $0\leq\theta\leq\pi$, the LLC converter gain at the parallel resonant frequency, f_p, will meet the PFC gain requirement ($0\leq\theta\leq\pi$) as per (18). In short, we only design the LLC at one phase $\theta=\pi/2$ to meet the PFC requirement, then the requirement for the other phase will automatically be satisfied.

$$M_{LLC}\left(f_s=f_p,\theta=\frac{\pi}{2}\right)$$

$$=\frac{1}{\sqrt{\left(\frac{K^2}{1+K}\right)}\cdot\left(\frac{\pi^2}{2}\cdot\frac{P_{out}}{V_{in\_RMS}^2}\cdot\sqrt{\frac{L_r}{C_r}}\right)}\geq 1 \qquad (16)$$

$$M_{LLC\_total}\left(f_s=f_p,\theta\right)\geq\frac{V_{out}}{\sqrt{2}V_{in\_RMS}}\cdot\frac{1}{(\sin\theta)^2} \qquad (17)$$

$$M_{LLC\_total}\left(f_s=f_p,\theta\right)\geq\frac{V_{out}}{\sqrt{2}V_{in\_RMS}}\cdot\frac{1}{(\sin\theta)^2}$$

$$\geq G_{req}\left(\theta\right)=\frac{V_{out}}{\sqrt{2}V_{in\_rms}}\cdot\frac{1}{\sin(\theta)} \qquad (18)$$

D. Extended LLC Resonant Converter Design Guideline for PFC with Wide Input and Output Voltages Requirements

The proposed design guideline can also be adapted to the PFC applications with a wide AC input voltage, $V_{in}^{min}\leq V_{in}\leq V_{in}^{max}$, and wide DC output voltage, $V_{out}^{min}\leq V_{out}\leq V_{out}^{max}$ as follows:

The LLC transformer ratio should be set based on the minimum gain requirement which occurs at the maximum input (V_{in}^{max}) and the minimum output (V_{out}^{min}), as shown in (19).

$$n=\frac{V_{in\_rms}^{max}}{\sqrt{2}V_{out}^{min}} \qquad (19)$$

To explore the design rule of LLC PFC under all the cases of the output voltage range, we define

$$V_{out}=\lambda V_{out}^{max} \qquad (20)$$

$$\frac{V_{out}^{min}}{V_{out}^{max}}\leq\lambda\leq 1 \qquad (21)$$

With the changing of V_{out}, the gain requirement for wide output voltage range PFC comes into a λ-related expression as shown in (20).

$$G_{req\_ext}(\theta,\lambda)=\frac{V_{out}^{max}}{\sqrt{2}V_{in\_rms}\sin(\theta)}\lambda \qquad (22)$$

According to (11) and (13) the LLC converter gain in λ-dependent form is obtained in (23), where $Q_{full\_load\_vomax}$ is the quality factor when the output voltage is at V_o^{max}.

$$M_{LLC\_total\_ext}(f_s,\theta,\lambda)=\frac{1}{2n_{ext}}\cdot M_{LLC\_ext}(f_s,\theta)$$

$$=\frac{1}{2n_{ext}}\cdot\frac{1}{\sqrt{\left[1+\frac{1}{K}\left(1-\frac{f_r^2}{f_s^2}\right)\right]^2\lambda^2+4(\sin\theta)^4\left[\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)Q_{full\_load\_vo max}\right]^2}}\lambda \qquad (23)$$

The total gain of LLC converter at the parallel resonant frequency, f_p, is derived by using (20) to replace V_{out} in (15).

$$M_{LLC\_total\_ext}\left(f_s=f_p,\theta,\lambda\right)=\frac{1}{2n_{ext}}M_{LLC\_ext}\left(f_s=f_p,\theta,\lambda\right)$$

$$=\frac{1}{\sqrt{\left(\frac{K^2}{1+K}\right)}\cdot\left(\frac{\pi^2}{2}\cdot\frac{P_{out}}{(V_{in}^{min})^2}\cdot\sqrt{\frac{L_r}{C_r}}\right)}\cdot\frac{V_{out}^{max}}{\sqrt{2}V_{in}^{min}}\cdot\frac{1}{(\sin\theta)^2}$$

$$=\frac{1}{\sqrt{\left(\frac{K^2}{1+K}\right)}\cdot\left(\frac{\pi^2}{2}\cdot\frac{\lambda\cdot V_o^{max}I_{out}}{(V_{in}^{min})^2}\cdot\sqrt{\frac{L_r}{C_r}}\right)}\cdot\frac{V_{out}^{max}}{\sqrt{2}V_{in}^{min}}\cdot\frac{1}{(\sin\theta)^2} \qquad (24)$$

It is observed from (24) that the total LLC converter gain at f_p is decreasing while the gain requirement is increasing with the increase of λ when $\frac{V_{out}^{min}}{V_{out}^{max}}\leq\lambda<1$. Therefore, we only need to check the LLC converter gain considering the highest output voltage (λ=1) (shown in (25)) and make sure it satisfies the gain requirement (shown in (26)).

$$G_{req\_driv}(\theta,\lambda=1)=\frac{V_{out}^{max}}{\sqrt{2}V_{in\_rms}^{min}}\cdot\frac{1}{\sin(\theta)} \qquad (25)$$

$$M_{LLC\_driv}(f_s,\theta,\lambda=1)$$

$$=\frac{1}{\sqrt{\left[1+\frac{1}{K}\left(1-\frac{f_r^2}{f_s^2}\right)\right]^2+4(\sin\theta)^4\left[\left(\frac{f_s}{f_r}-\frac{f_r}{f_s}\right)Q_{full\_load\_vo max}\right]^2}} \qquad (26)$$

By following the derivation steps in II. C, the extended LLC resonant converter design guideline is obtained as follows:

a) the transformer turns ratio value is designed to be equal to $V_{in\_RMS}^{max}/\sqrt{2}\,V_{out}^{min}$

b) the gain of the LLC resonant tank at f_p is higher than the product of the variation ratios of input voltage and output voltage, considering the case $\theta=90°$ when line voltage is at peak value.

$$M_{LLC\_ext}\left(f_s=f_p, \theta=\frac{\pi}{2}\right) = \frac{1}{\sqrt{\left(\dfrac{K^2}{1+K}\right)\cdot 2Q_{full\_load\_vo\max}}} \tag{27}$$

$$\geq \frac{V_{in\_rms}^{\max}}{V_{in\_rms}^{\min}} \times \frac{V_{out}^{\max}}{V_{out}^{\min}}$$

III. Design Example

A 240 W, single-stage half-bridge LLC LED driver was designed and built using the proposed mathematical guideline. The specifications are shown in Table I.

TABLE I. SINGLE-STAGE LLC LED DRIVER SPECIFICATIONS

V_{in}	V_{LED}	I_{LED}	P_o	f_{line}
180~300 Vac	40~60 Vdc	4 A	240 W	60 Hz

The expected transformer turns ratio for the half-bridge LLC LED driver *n* is calculated in (28).

$$n = \frac{N_{pri}}{N_{sec}} = \frac{V_{in\_RMS}^{\max}}{\sqrt{2}V_{out}^{\min}} = \frac{300}{\sqrt{2}\cdot 40} \approx 5.3 \tag{28}$$

Table II lists the minimum gain requirement value for the desired LLC LED driver, calculated in (29).

TABLE II. LLC TANK GAIN REQUIREMENT AT THE PARALLEL RESONANT FREQUENCY (F_P)

$M_{LLC}(f_p)$	V_{out_max}	I_{o_max}	$P=p(\theta=\pi/2) = 2P_o=2V_{out}^{max}\times I_{out}$
>2.5	60 V	4 A	2×60 V×4 A=480 W

$$\frac{V_{in}^{\max}}{V_{in}^{\min}} \times \frac{V_{out}^{\max}}{V_{out}^{\min}} = \frac{300}{180} \times \frac{60}{40} = 2.5 \tag{29}$$

The key LLC parameters are listed in Table III.

TABLE III. KEY PARAMETERS OF DESIGNED SINGLE-STAGE LLC LED DRIVER

N_{pri}:N_{sec}	11:2
Transformer Core	PQ 40
L_m	103 µH
L_r	20 µH
C_r	FKP1O116804D00JSSD×3 (6800 pF 1 KV)
Output capacitor C_o	B43504A2108M×3 (1000 µF, 250 V)
Switching frequency(f_s)	100 kHz ~ 250 kHz
Switches (S_H & S_L)	SPP11N80C3

As shown in Fig. 4, the designed LLC resonant tank features a normalized gain of 2.72 at the parallel resonant frequency fp/fr=0.392, which is 9% higher than the requirement of 2.5. According to the proposed extended LLC PFC design guideline, once the LLC gain meets the PFC requirement at peak AC input voltage, it will meet the requirement for the entire line voltage cycle.

This is demonstrated in Fig. 5, where the resulting gain curve for the designed LLC PFC (in green) crosses the gain requirement (in red) only at $\theta=90°$ when $p_{out}(\theta)=2P_o$ (the output power curve is shown in blue), and then is always higher than the requirement when $0<\theta<180°$, $0<p_{out}(\theta)<2P_o$. Fig. 6 also shows that the designed LLC gain (the colored surface) is always higher than the PFC gain requirement (the red surface) within the specified output voltage range (*40 V<V_{out}<60 V, 0<θ< π*), resulting in a successful LLC PFC design.
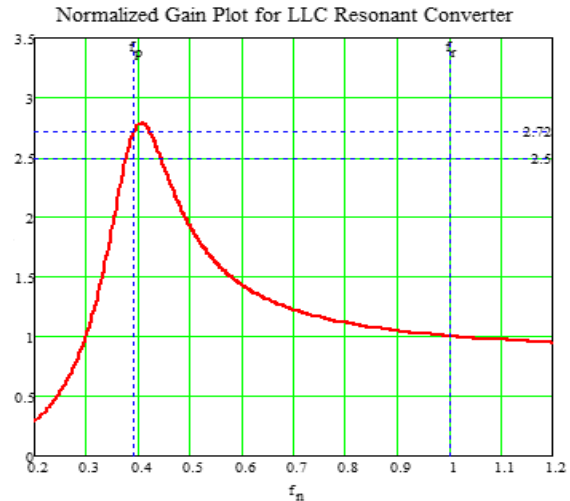

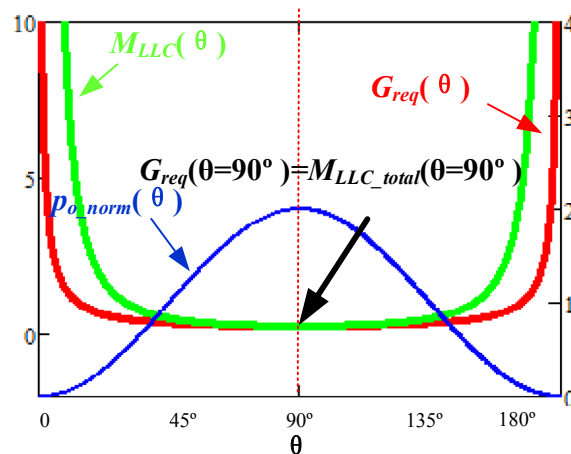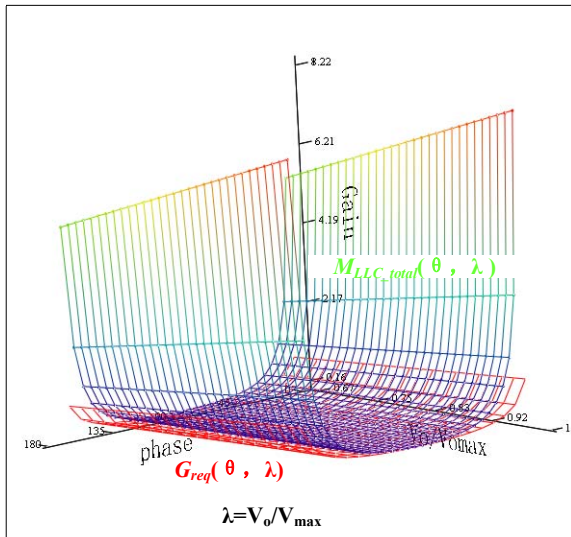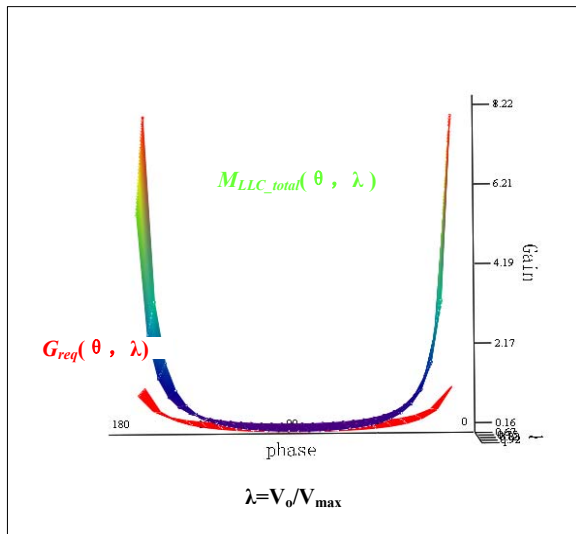Fig. 4. Normalized Gain Plot of the Designed LLC Resonant Converter at heaviest load $p_{out}(\theta=90°)=2P_O$

Fig. 5. Gain Requirement vs. Gain Curve of the Designed LLC Resonant Converter Considering $V_{out}=V_{out}^{max}=60$ V

Considering the entire operating range of output voltage, a 3-D surface plot is drawn in Fig. 6 using the PFC gain requirement expression in (22) and the LLC gain expression at parallel resonant frequency in (24). The gain requirement is a red surface, while the LLC gain is an irregular colored surface. Both of them are changing with $\lambda=V_o/V_o^{max}$ and phase of line voltage θ. It is observed that the designed LLC resonant tank features the gain that is always higher than the requirement within the specified output voltage range as

well as the entire half line voltage cycle ($0.667 < \lambda < 1$, $0° < \theta < 180°$), resulting in a successful LLC PFC design.

$M_{LLC\_driv\_total}, G_{req\_driv}$

$M_{LLC\_driv\_total}, G_{req\_driv}$

Fig. 6. Designed LLC Resonant Converter Gain vs. PFC Gain Requirement in 3D Surface Plot Considering the Wide Output Voltage ($V_{out}^{min} < V_{out} < V_{out}^{max}$)

IV. EXPERIMENTAL VERIFICATION

The pictures of the designed 240W single-stage half-bridge LLC LED driver prototype is shown in Fig. 7 while the LED load is shown in Fig. 8. The load is made of 2 paralleled-connected LED bars and each LED bar has 18 pieces of LED chips from Cree (XMLBWT-02-0000-0000T5051CT) connected in series to provide enough load ability (the LED voltage up to 60V and LED current up to 4A).

Fig. 7. 240W Single-Stage LLC PFC LED Driver Prototype

Fig. 8. 240W LED Lamp Load (V_{LED}=40~60V, I_{LED}=4A)

As shown in Fig. 9, the PFC control strategy is implemented using dsPIC33FJ32GS606. A linear opto-coupler is used to transmit LED current signal to the primary side. The LED current signal is sampled by an ADC, and then subtracted from a reference voltage value to create an error value. The error value is processed by a slow PI controller and becomes one of the two essential signals to create the input current reference. The other essential information for the input current reference is the sinusoidal input voltage. The rectified input voltage is firstly scaled down to adapt the DSC analog input range and then sampled by the second ADC. By multiplying the error value from the first ADC and the scaled input voltage reference from the second ADC, a rectified sinusoidal input current reference signal is generated.

Since it is difficult to accurately obtain the average input current value over one switching cycle in LLC resonant topology due to the irregular current waveform and the existence of circulation current, the input current value is calculated by using the cycle-by-cycle average input current sensing method proposed in [14]. This method accurately measures the average input current over each switching period by sensing the series resonant capacitor voltage and the input voltage at a particular time instant and thus provides real-time average input current information.
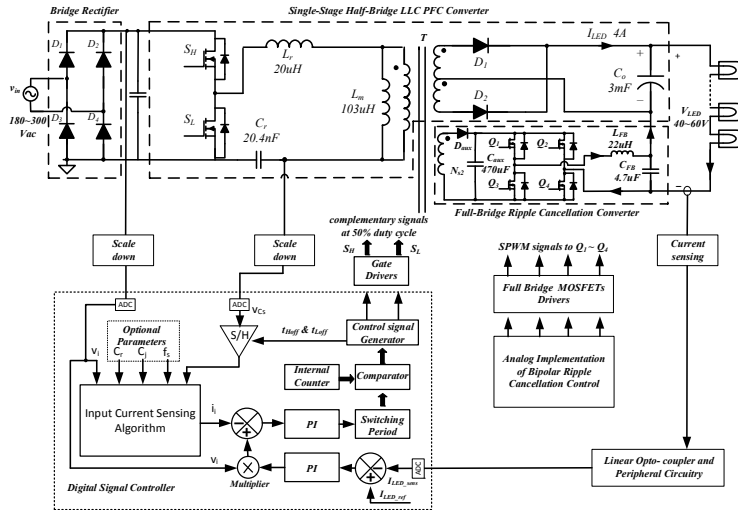
Fig. 9. The Implementation of the Single-Stage LLC Resonant LED Driver.

The experimental prototype presents power factor performance of 0.99 at 180 V AC input, as shown in Fig. 10. It is noticed that there are "a blank portions" of input current in the vicinity of the input voltage zero crossing points. This is caused by the nonlinearity of the MOSFET output capacitance, C_{oss}, which is a nonlinear capacitance that varies with the drain-to-source voltage of the MOSFET[15]. As an average C_{oss} value is used in the existing digital implementation, the nonlinearity of C_{oss} value in the real circuit results the sensing error at the light input current and the low input voltage. The existing prototype is using Si MOSFET (SPP11N80C3) as the half bridge switches, featuring quite high C_{oss} value at low input voltage ($C_{oss@Vin=30V}$>500pF). Using the GaN HEMTs with significantly reduced C_{oss} ($C_{oss@Vin=30V}$<150pF) will reduce the difference between the average value and the real value of C_{oss} and lead to the improved PF performance.
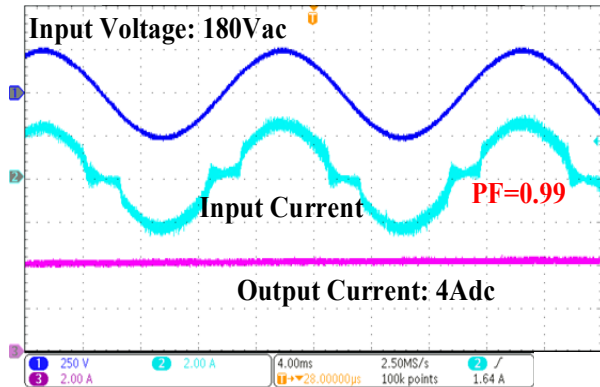
92% is achieved. The 120 Hz output ripple is cancelled by an auxiliary ripple cancellation circuit [16, 17]. The PF and efficiency data under different input and output voltages are shown in Fig. 18 and Fig. 19.
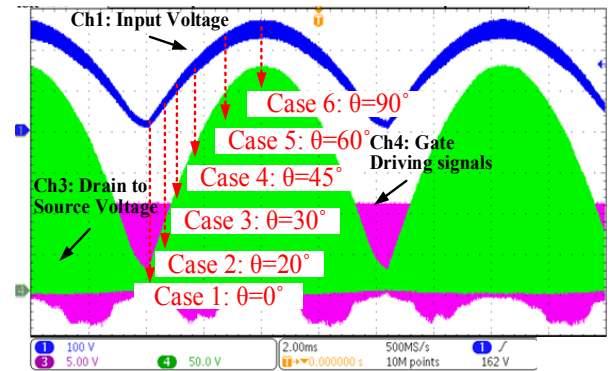

Fig. 11. Soft Switching Performance of the LLC PFC on Primary Side at Different Phase Angle, When V_{in}=180 Vac, V_{LED}≈60 V, I_{LED}=4 A, P_O=240 W

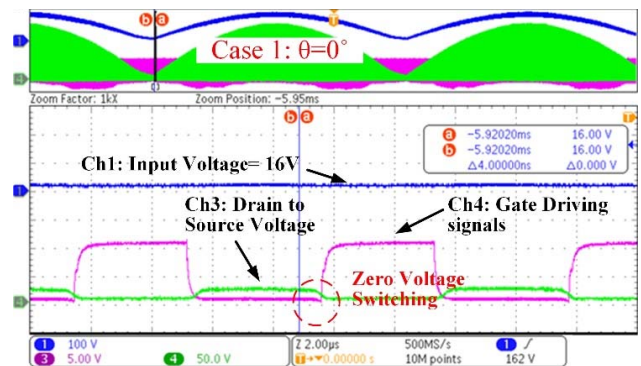Fig. 10. Power factor performance of the Half-bridge LLC LED Driver, When V_{in}=180 V, I_{out}=4 V, V_{out}≈60 V

Zero voltage switching performance during the whole PFC operation are shown in Fig. 11 ~ Fig. 17. Also, the design presents a cost-effective, high-efficiency solution, compared with the two-stage LED driver solution. A peak efficiency of

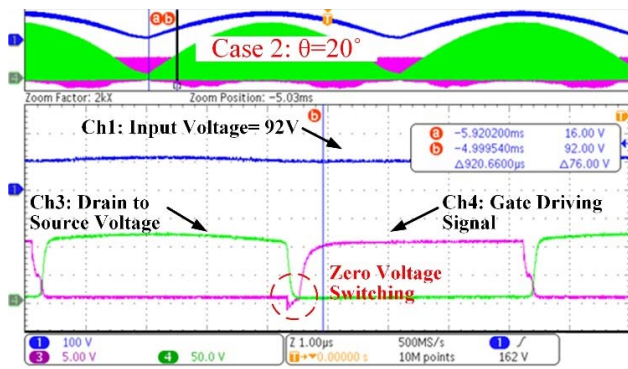Fig. 12. ZVS Performance of the LLC PFC on Primary Side at θ=0º, When V_{in}=180 Vac, V_{LED}≈60 V, I_{LED}=4 A, P_O=240 W

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Fig. 13. ZVS Performance of the LLC PFC on Primary Side at θ=20º, When V_{in}=180 Vac, V_{LED}≈60 V, I_{LED}=4 A, P_O=240 W
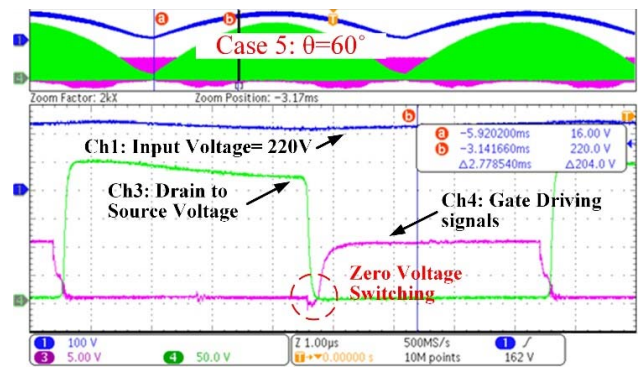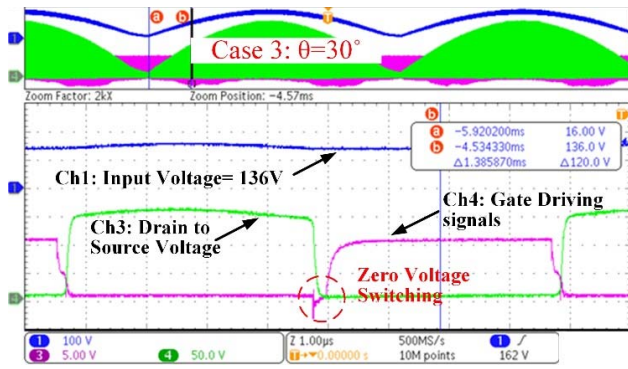

Fig. 14. ZVS Performance of the LLC PFC on Primary Side at θ=30º, When V_{in}=180 Vac, V_{LED}≈60 V, I_{LED}=4 A, P_O=240 W

Fig. 15. ZVS Performance of the LLC PFC on Primary Side at θ=45º, When V_{in}=180 Vac, V_{LED}≈60 V, I_{LED}=4 A, P_O=240 W

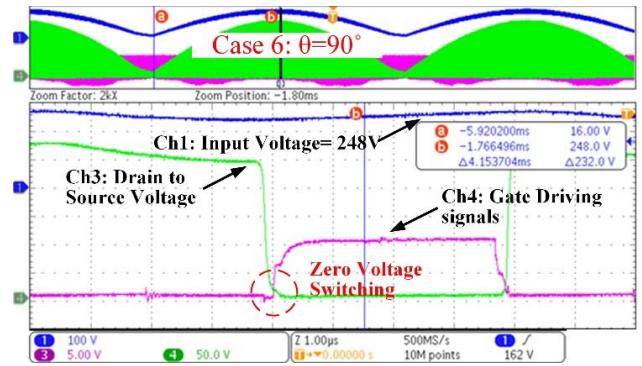Fig. 16. ZVS Performance of the LLC PFC on Primary Side at θ=60º, When V_{in}=180 Vac, V_{LED}≈60 V, I_{LED}=4 A, P_O=240 W

Fig. 17. ZVS Performance of the LLC PFC Stage on Primary Side at θ=90º, When V_{in}=180 Vac, V_{LED}≈60 V, I_{LED}=4 A, P_O=240 W
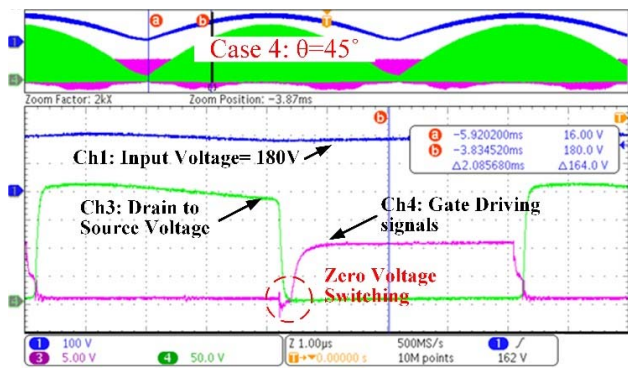

Fig. 18. Power factor performance of the Half-bridge LLC LED Driver at Different Input and Output Voltages
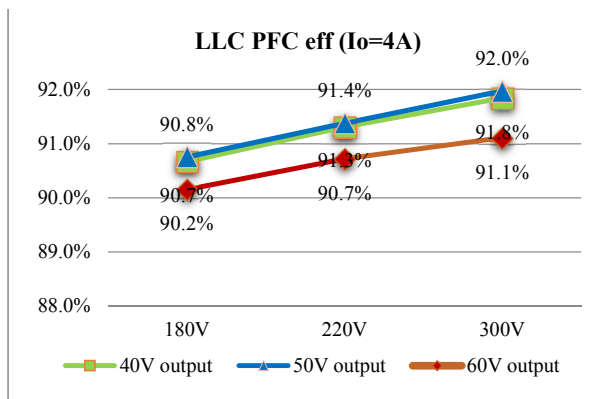
LLC PFC eff (Io=4A)

Fig. 19. Efficiency of the Half-bridge LLC LED Driver at Different Input and Output Voltages

CONCLUSION

In this paper, a mathematical LLC-type converter design guideline for PFC is proposed, which is intuitive and easy to apply. By carefully designing the LLC resonant converter with its tank gain at parallel resonant frequency to be higher than 1 considering the case when line voltage is at peak value, its gain will meet the single-stage PFC requirement for the entire line voltage range (0<θ<180º), resulting in a successful LLC PFC design. To verify the design rule and demonstrate the advantages of the single-stage LLC power factor correction topology, a 240W offline high power LED driver is built with variable input voltage range 180Vac~300Vac and variable output voltage range of 40Vdc~60Vdc. Featuring a high peak power factor performance of 0.99, the design presents a cost effective and high-efficiency solution, compared to the conventional two-stage LED driver solution. A peak efficiency of 92% has been achieved on the prototype.

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